REMARKS

Claims 1-42 were pending in the present application. Claims 1-3, 10, 12, 16-18, 24, 26-30, 33, 36, 37, 39, and 40 have been amended. Accordingly, claims 1-42 remain pending in the application.

Claims 1-9, 12-42 stand rejected under 35 U.S.C. §102(b) as being anticipated by Hunter et al. (U.S. Patent No. 5,394,555) (hereinafter "Hunter"). Although Applicant respectfully traverses this rejection, Applicant has amended the claims for clarity.

Claim 10 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Hunter in view of Farmwald et al. (U.S. Patent No. 5,606,717) (hereinafter "Farmwald"). Although Applicant respectfully traverses this rejection, Applicant has amended the claims for clarity.

Claim 11 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Hunter in view of Baxter et al. (U.S. Patent No. 5,887,146) (hereinafter "Baxter"), and in further view of Martin et al. ("Bandwidth Adaptive Snooping") (hereinafter "Martin"). Applicant respectfully traverses this rejection.

Applicant's claim 1 recites a system comprising in pertinent part,

> "wherein an active device included in a node of the plurality of nodes is configured to initiate a write back transaction involving a coherency unit by sending either a first type of address packet or a second type of address packet on the address network dependent on whether the active device is included in a multi-node system." (Emphasis added)

The Examiner asserts Hunter teaches each and every limitation recited in Applicant's claim 1. Applicant respectfully disagrees with the Examiner's characterization of Hunter and the application of Hunter to Applicant's claims. More particularly, the Examiner asserts Hunter teaches at col. 4, lines 20-25, the active device sending a first or a second type of address packet depending on whether the node is in a

multi-node network. Applicant disagrees. Specifically, Hunter actually teaches at col. 4, lines 9-25

> "The DSBA is an environment which offers the simplest way to understand the real-time operation of SOs. Referring to FIG. 2, each node in the cluster (only two nodes of two CPUs 1 each are shown for simplicity) contains an **External Coherency Unit (ECU)** 10 that: (a) snoops its own node-local bus 4 for commands on shared cache-lines that are also present in other nodes, and (b) conditionally forwards these commands (using a unique identifier for the cache-line) to the other nodes via, for example, a separate inter-node ECU bus 11. (Point-to-point connections are also possible, using a directory in each ECU to keep track of which nodes have copies.) All other **ECUs**: (a) snoop the inter-node ECU bus 11 for commands that affect cache-lines resident in their own local memories, (b) translate these to their own physical tags and (c) inject the translated commands into their own node-local buses." (Emphasis added)

From the foregoing, it is clear that Hunter is teaching the CPU (active device) sending one type of command within the node, and the ECU (interface) translating the command and then sending different commands external to the node based upon snooping traffic on the various internal and external buses. Furthermore the ECU sends the different command dependent upon whther the cache line is present in another node, not whether there is another node present. This is not the same as a given CPU in a node sending on an internal bus one type of address packet (command) if it is in a multinode system, and a different type of address packet if it is not in a multinode system.

Accordingly, Applicant submits Hunter does not teach or disclose "wherein an active device included in a node of the plurality of nodes is configured to initiate a write back transaction involving a coherency unit by sending either a first type of address packet or a second type of address packet on the address network dependent on whether the active device is included in a multi-node system," as recited in claim 1.

In regard to the rejection of claim 10, the Examiner asserts Hunter teaches the owner of a node providing data about a coherency unit at col. 6, lines 31-40, and acknowledges Hunter does not teach the use of a NACK packet. The Examiner further asserts Farmwald teaches the use of a NACK packet. Applicant respectfully disagrees

with the Examiner's characterization of Hunter. More particularly, at col. 31-40 Hunter actually discloses at col. 6, lines 21-40

> "For example, if a CPU wishes to obtain an exclusive copy of a shared cache-line, it places a suitable command (e.g., RTW--"read with intent to write"--in the exemplary system to be explained more fully below) on its node-local bus which will cause **each ECU 10** to take the following set of possible actions:
> (1) if the cache-line state is exclusive or modified, it will be retrieved directly from local memory 3 and sent to the requesting processor with no remote action taken because no other copies exist;
> (2) if the state is invalid, an RTW command will be transmitted over the inter-node ECU bus 11 to other nodes. A remote node that contains the line in exclusive or modified state will transmit (siphon) the cache line over the inter-node ECU bus to the requester. If several nodes contain the line in the shared state, all attempt to send it, but ECU bus conventional priority logic will choose one and cancel the others. All remote copies will be set to the invalid state." (Emphasis added)

From the foregoing, it is clear Hunter is merely teaching a CPU requesting a cahe line locally, and an ECU retrieving the data and providing oit to te requester if it is modified or exclusive. If the cache line is invalid the RTW commnad is sent over the ECU bus to other nodes, and some other node that has the cache line will send the data back to the requester. if several nodes have te cache line in the shared state, they may all try to send it but the ECU will choose one and cancel the others. Applicant fails to see how this teaches a

Accordingly, in contrast to the Examiner's assertion Hunter does not teach or disclose "wherein the active device is configured to send the RWB address packet **if** the active device is included in a multi-node system and the WB address packet if the active device is included in a single node system;" "wherein if the active device sends the RWB address packet and another active device included in the node gains ownership of the coherency unit before an interface included in the node sends a responsive address packet, the other active device is configured to provide data to the interface in response to the responsive address packet;" or "wherein if the active device sends the WB address packet and the other active device included in the node gains ownership of the coherency unit before a memory subsystem included in the node sends a different responsive

address packet, the active device is configured to send a NACK data packet to the memory subsystem," as recited in claim 10.

Thus for the foregoing reasons, Applicant submits claim 1 along with its dependent claims, patentably distinguishes over Hunter, and over Hunter in view of Farmwald, Baxter, and Martin.

Applicants claims 16 and 28 recite features that are similar to the features recited in claim 1. Accordingly, Applicant submits claims 16 and 28, along with their respective dependent claims, patentably distinguish over Hunter, and over Hunter in view of Farmwald, Baxter, and Martin for at least the reasons given above.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-13301/SJC.

Respectfully submitted,

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